



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,041	11/17/2003	Min Cao	PS-62A	1040
23933	7590	06/03/2004	EXAMINER	
STUART T AUVINEN			CAO, PHAT X	
429 26TH AVENUE			ART UNIT	
SANTA CRUZ, CA 95062-5319			PAPER NUMBER	
			2814	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/707,041

Applicant(s)

CAO, MIN

Examiner

Phat X. Cao

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-6 is/are allowed.
- 6) ☒ Claim(s) 7-10 is/are rejected.
- 7) ☒ Claim(s) 11 and 12 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

## Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

## DETAILED ACTION

### *Claim Objections*

1. Claim 7 is objected to because of the following informalities: in claim 7, line 19, "a inversion layer" should be changed to "an inversion layer". Appropriate correction is required.

### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 7-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Gallagher et al (US. 3,562,608).

Regarding claim 7, Gallagher (Figs. 2 and 3) discloses a gated-diode variable capacitor comprising: a gate 22 formed over a thin insulator 17 that separates the gate 22 from a substrate 10; a source 14 formed in the substrate on a source side of the gate; a substrate tap 16 for connecting a substrate bias voltage to a substrate 10 under the gate; an upper-gate contact to the gate 22 for applying an upper voltage 34 to an upper portion of the gate; and a lower-gate contact to the gate 22 for applying a lower voltage ground to a lower portion of the gate; wherein the upper voltage 34 is higher than the ground lower voltage, wherein a gate-to-source varies along the gate (column 2, lines 20-26); wherein a source bias voltage 26 applied to the source 14, the upper voltage 34 and the lower voltage ground cause an inverted portion of the gate to have

an inversion layer 36 formed in the substrate under the inverted portion, and a non-inverted portion of the gate to not have an inversion layer formed in the substrate under the non-inverted portion (Fig. 3 and column 2, lines 26-50); wherein a capacitance per unit area of the inverted portion is higher than a capacitance per unit area of the non-inverted portion (column 2, lines 69-75 through column 3, lines 1-5); wherein capacitance of the variable capacitor measured from the source to the substrate is adjustable by adjusting a ratio of an area of the inverted portion to the area of the non-inverted portion, whereby capacitance is adjustable by adjusting areas of inverted and non-inverted regions under the gate (Fig. 3 and column 2, lines 69-75 through column 3, lines 1-11).

Regarding claim 8, Gallagher's Fig. 2 further discloses: the substrate bias voltage 16 is connected to ground, the substrate 10 is a p-type substrate, the upper voltage 34 is more than a transistor threshold above the source bias voltage ground, but the lower voltage is less than the transistor threshold above the source bias voltage (column 2, lines 26-50).

Regarding claim 9, Gallagher's Fig. 2 further discloses: a variable voltage generator 32 coupled to the upper-gate contact and to vary the upper voltage 34 applied to the gate 22; wherein the lower voltage is ground.

#### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al (US. 3,562,608).

Gallagher's Fig. 2 further discloses a variable voltage generator 28 coupled to the source 14 by a source contact, to vary the source bias voltage 26 applied to the source. Gallagher's Fig. 2 also discloses a variable voltage generator 32 coupled to the upper-gate contact, but no disclose a fixed voltage generator coupled to the upper gate contact.

However, it would have been obvious to couple either a fixed voltage generator or a variable voltage generator to the upper-gate contact because this change would not be effect in the varying the channel-to-substrate capacitance of the device. In the other words, the varying the channel-to-substrate capacitance of Gallagher's device would be the same by varying the variable voltage source generator 28.

***Allowable Subject Matter***

6. Claims 1-6 are allowed.

The prior art of record fails to disclose the combination of a variable capacitor Structures recited in the base claim, including the combination of a structure comprising: variable voltage means for generating a first voltage that can be varied to adjust a capacitance value of the variable capacitance; and multi-voltage means, coupled between the variable voltage means and a second voltage, for generating a plurality of voltages between the first and second voltages; wherein the plurality of voltages are each applied to a different one of the gate segments whereby the gate segments are

biased to a plurality of differing gate segment biases between the first and second voltages, whereby the capacitance value at the first terminal means is increased by adjusting the first voltage, causing additional gate segments to form conducting channels that increase capacitance.

7. Claims 11-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record fails to disclose the source and the drain are both coupled to the source bias voltage (claim 11), and fails to disclose the gate comprises a plurality gate arms biased to different voltages between the upper voltage and the lower voltage, wherein gate current flow is blocked by electrical isolation of the gate arms.


8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phat X. Cao whose telephone number is (571) 272-1703. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Art Unit: 2814

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PC  
May 28, 2004

  
PHAT X. CAO  
PRIMARY EXAMINER